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Privacy Protection of VLSI Circuits through High Level Transformation Based Obfuscation

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Abstract: *For any semiconductor manufacturing requires greater capital investments, the use of contract foundries has grown dramatically, increasing exposure to theft and unauthorized excess production. Many recent activities proved that IC piracy has now become a major challenge for the electronics and defense industries. In this paper we presents a novel approach to design obfuscated circuits for digital signal processing (DSP) applications using high-level transformations, a key-based obfuscating finite-state machine (FSM), and a reconfiguration. The goal is to design DSP circuits that are harder to reverse engineer. With several modes of operations for obfuscation where the outputs are meaningful from a signal processing point of view, but are functionally incorrect for better confusion. The configure data controls various modes of the circuit operation and Functional obfuscation is accomplished with the use of the correct initialization key. Structural obfuscation is also achieved by the proposed methodology via high-level transformations. The efficiency of proposed methodology is verified with FIR design, strong high level obfuscation is proved and analyzed for various key sizes.*

I. INTRODUCTION

The problem of hardware security is a serious concern that has led to a lot of work on hardware prevention of piracy and intellectual property (IP) [1], which can be broadly classified into two main categories: 1) authentication-based approach, or 2) obfuscation-based approach. Obfuscation-based approach [1] is of interest in this paper, which is a technique that transforms an application or a design into one that is functionally equivalent to the original but is significantly more difficult to reverse engineer. Some hardware protection methods are achieved by altering the human readability of the Hardware description language (HDL) code, or by encrypting the source code base cryptographic techniques. Recently, a number of hardware protection schemes have been proposed that modify the finite-state machine (FSM) representations to obfuscate the circuit's .However, to the best of our knowledge, no obfuscation based IP protection approach has been proposed for DSP circuits [1] in the literature. This paper, for the first time, presents design of obfuscated DSP circuits via high-level transformations that are harder to reverse engineer. From this standpoint of view, a DSP circuit is more secure, if it is harder for the adversary to discover its functionality. In other words, a high level of security is achieved if the functionality of a DSP circuit is designed to be hidden to the adversary our goal is to design obfuscated circuits by applying high-level transformations during the design phase. The key idea of the proposed work is to generate meaningful design variations by exploiting high-level transformations [4]. A critical challenge for nano electronic systems is to achieve yield and reliability. As VLSI technology scales into the nanometer scale, devices and interconnects are subject to increasingly prevalent defects and significant parametric variations. Based on photolithography, we are making layout features of smaller dimensions than the wavelength of the light, which requires increasingly complex OPC and other DFM techniques [3] at increasing layout area cost. Future nano electronic systems are expected to be based on self-assembly manufacture of physical structure, and achieve. Reconfiguration is further critical for nano electronic systems [5] to achieve yield and Reliability by bypassing defective or degraded devices and interconnects [4], which occurrence cannot be avoided or reduced below a certain level as is determined by the uncertainly principle of quantum physics .In this paper, we present that reconfigurable computing [2] is further a critical technology to achieve hardware security in the presence of supply chain adversaries. In recent years, a growing number of software based security solutions have been migrated to hardware-based security solutions for much enhanced resistance to software based security threats. Such systems range from smartcards to specialized secure co-processing boxes, wherein hardware provides the source of security and trust for a number of security primitives. However, in recent years, it has been brought into light that hardware is also subject to a number of security threats. The existing techniques mostly focus on information leak from a hardware system: An adversary may extract cryptographic keys and confidential information from a system by testing reverse engineering , or side-channel analysis . Design Automation and Test in Europe (DATE) [2] , 2014. Bao Liu is with the University of Texas,

San Antonio, TX, 78249. Brandon Wang is with Cadence Design Systems, Inc, San Jose, CA, 95134 . In today's global IC industry, a supply chain adversary, such as an IP provider, an IC design house, a CAD company, or a foundry may have access to the source code of the design, and may easily tamper a hardware system by planting time bombs which compromise hardware computation integrity, or creating back doors which enable information leak, bypassing access control mechanisms at higher (e.g., OS and application) levels. The recently-released Comprehensive National Cyber Security Initiative has identified this supply chain risk management problem as a top national priority A supply chain adversary's capability is rooted in his knowledge on the hardware design. Successful hardware design obfuscation would severely limit a supply chain adversary's capability if not preventing all supply chain attacks. **Section II** to show resent trents of hardware intellectual property(IP) piracy and reverse engineering. **Section III** DSP hardware protection methodology through obfuscation by hiding functionality via high level transformations. **Section IV** to implement simulation verified. **Section V** to verified different value FSM modes and reduced area

II. HIGH LEVEL TRANSFORMATION

A supply chain adversary is an insider who is involved in the design and manufacturing of a hardware device. The tamper capability is based on his role in the supply chain, specifically, his read and write permission in the design and the manufacturing process of a specific device. An IP provider [4] or a designer for a specific module may have limited access to the design, while a foundry or a chip-level integration designer has access to the whole device design. The general lack of access control in today's supply chain further facilitates an adversary to gain knowledge of a design and launch attacks. Besides based on his role in the supply chain, a supply chain adversary may gain further knowledge of a design by probing, testing, side-channel analysis, or reverse engineering. The state-of-the-art VLSI logic encryption/locking techniques [2] include combinational logic locking and finite-state machine (FSM) locking. Combinational logic locking augments a combinational logic network [3] with an additional group of lock inputs such that the augmented combinational logic network has the same function as the original combinational logic network only if a specific vector (aka a valid key) is applied to the lock inputs .The simplest combinational logic locking technique is to insert XOR and XNOR gates into a combination logic network . An adversary knows which inputs are functional inputs and which inputs are lock inputs. He can then identify the lock gates connected to the lock inputs. If a total of M lock gates are inserted in a combinational logic network, the complexity for an adversary to find the correct logic may not be 2 M . Another combinational logic locking technique is to insert multiplexers or combine logic functions based on Shannon expansion. The reason is as follows. If a lock input is connected to a lock gate that is not a XOR or XNOR gate, the key to the lock input is implied to be the non-controlling logic value of the lock gate An adversary can then easily obtain the key, unless the lock input is connected to multiple lock gates and is implied to have conflicting logic values - for example, the lock input is connected to a group of AND gates and a OR gate which have the same function as a XOR or XNOR gate. Recent trends of hardware intellectual property (IP) piracy and reverse engineering pose major business and security concerns to an IP-based system-on-chip (SoC) design flow we propose a Register Transfer Level (RTL) hardware IP protection technique based on low-overhead key-based obfuscation of control and data flow. The basic idea is to transform the RTL core into control and data flow graph(CDFG)and the integrate a well obfuscated finite state machine (FSM) of special structure, referred as" Mode-Control FSM" ,into the CDFG in a manner that normal functional behavior is enabled only after application of a specific input sequence.

III. DESIGN FLOW OF THE PROPOSED DSP CIRCUIT OBFUSCATION APPROACH

A novel DSP hardware protection methodology through obfuscation by hiding functionality via high-level transformations. This approach helps the designer to protect the DSP design [5] against piracy by controlling the circuit configuration among the generated variation modes F G SR clkReconfigurator reset re-set state M U X . . . select signal connection 1 connection 2 connection k Obfuscating configuration FSM key (switch instances)

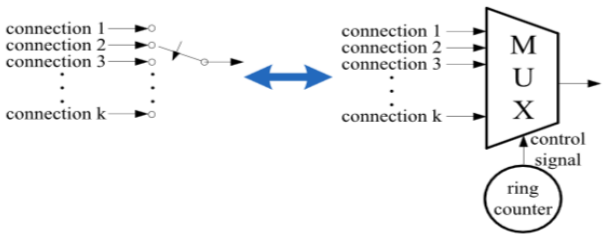


Fig.1 Proposed secure switch design of the original design

The detailed design flow is described below:
Step 1: DSP algorithm. This step generates the DSP algorithm based on the DSP application [3]
Step2: High-level transformation selection. Based on the specific application, appropriate high-level transformation should be chosen according to the performance requirement (e.g., area, speed, power or energy).
Step 3: Obfuscation via high-level transformation. Selected high-level transformations are applied simultaneously with obfuscation where variation modes, and different configurations of the switch instances are designed.
Step 4: Secure switch design. The secure switch is designed based on the variations of high-level transformations. Note that different configure data could be mapped into the same mode, which only involves simple combinational logic synthesis.
Step 5: Two-level FSM generation. The reconfigurator and the obfuscating FSM are incorporated into the DSP design as shown in Fig2. The configuration key is generated at this step.
Step 6: Design specification. This step includes the HDL and netlist generation and synthesis of the DSP system. The proposed design methodology does not require significant changes to established verification and testing flows. In fact, the obfuscated DSP circuit with the correct key behaves just like the original circuit.

a) Secure switch design

Here we use that the DSP circuits can be obfuscated via high-level transformations by appropriately designing the switches in a secure manner. The switches generated by high-level transformations are periodic N-to-1 switches. These switches can be implemented as multiplexers, whose control signals are obtained from ring counters (as shown in Fig 2.Thus, the security of the switch relies upon design of the ring counters such that the outputs of the ring counters can be obfuscated. A ring counter is often modeled as an FSM. An FSM is usually defined by a 6-tuple (I, O, S, S0, F,G), where is a finite set of internal states, I and O represent the inputs and outputs of the FSM, respectively, F is the next-state function, G is the output function, and S0 is the initial state. However, unlike general FSMs, the FSM [2] of a ring counter is input independent, such that it always transits to the next state based on the current state. As a result, the control signal of the switches (i.e., output of the FSM) will be periodic.

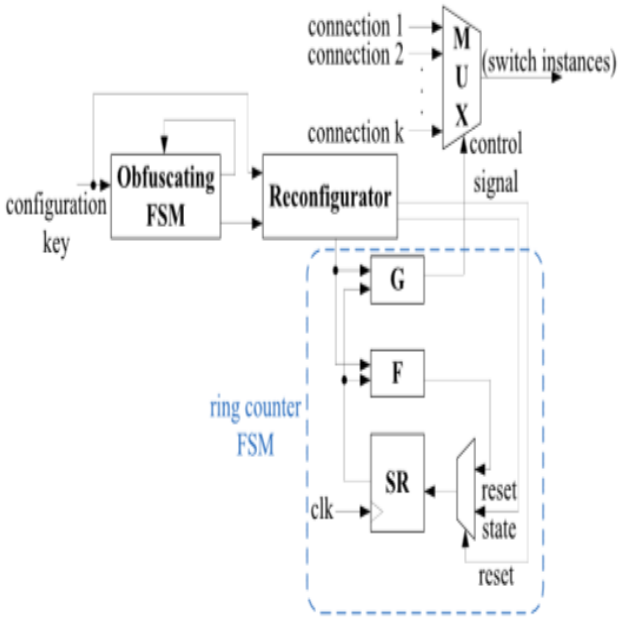


Fig 2 Complete reconfigurable switch design

b) Reconfigurable Switch Design

In existing works have demonstrated that functional obfuscation can be achieved by embedding a well-hidden FSM (i.e., obfuscating FSM) in the circuit to control the functionality based on a key. In order to achieve design obfuscation by using high-level transformations, we propose a reconfigurable switch design. The detailed implementation is shown in Fig. 3, where SR represents the state registers that store the information of the current state [4]

c) Proposed methodology

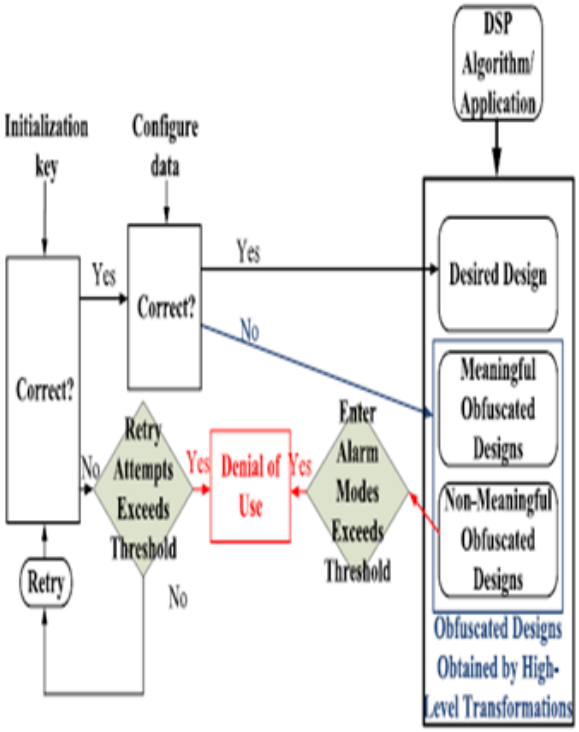
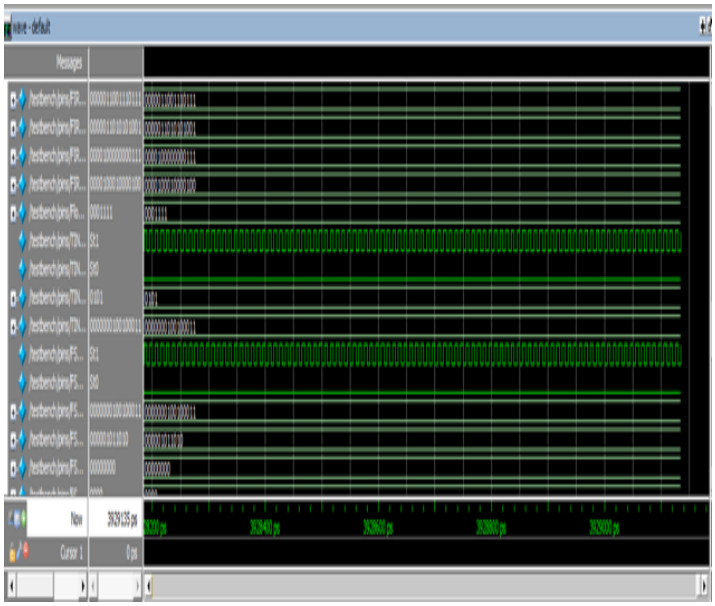


Fig. 3 proposed methodology diagram

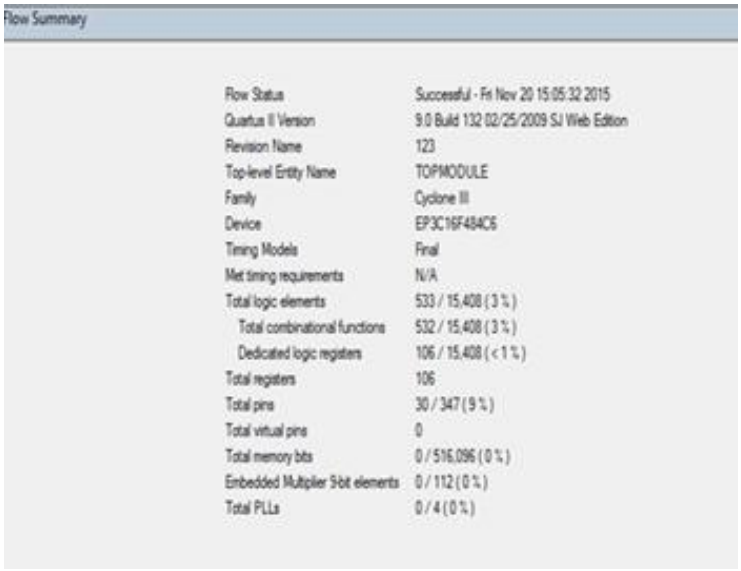
High-level transformations also allow design of circuits using same data path but different control circuits. For example, a data path may implement a 3rd-order or a 6thorder digital filter, or in general a (3l) th-order filter, where l is a positive integer. These correspond to different modes. While these modes generate outputs that are functionally incorrect, these may represent correct outputs under different situations, since the output is meaningful from a signal processing point [5] of view. Finally, other modes lead to non-meaningful outputs. The initialization key and the configure data must be known for the circuit to work properly. Consequently, the circuit behaves as an obfuscated circuit.

IV. SOFTWARE IMPLEMENTATION RESULTS

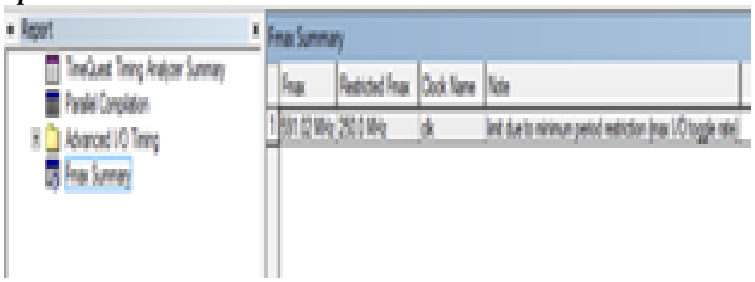
a) Functional verification in Modelsim



b) Performance of area



c) Performance of speed



d) Power analyzer

e) comparision table

SBOX TYPE	AREA	SPEED
TYPE1	**533**	**328.62MHz**
TYPEII	**512**	**63.76MHz**
TYPEIII	**512**	**341.53MHz**

V. CONCULSION

This paper presents a low- over head solution to design DSP circuita that are obfuscated both structurally and functionally by utilizing High Level Transformations techniques.It is shown that verifying the equivalence of DSP circuits by employing High Level Transformations will be harder if some switches can be

designed in such a way that are difficult to trace, A secureconfigurable switch design is incorporated int the proposed design scheme to improve the security.A complete design flow is presented in the proposed obfuscation methodology the variation modes and the additional obfuscating circuits could also be designed systematically based on the High Level Transformations.obfuscated and reconfigure FSM modes of which reduces the area of performance speed improved to 341.53MHZ.

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